The Technology Development on Further Enhancing the Cost Performance of Multi-crystalline Silicon Wafers.

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The Challenge from Mono-Crystalline Si Technology

- **Low Power Consumption**
  - 35 ~ 50 Kw (24” ~ 26” hot zone)
  - Around 6% reduction of crystal cost

- **High Pulling Speed**
  - 1.3 ~ 1.5 mm/min
  - Around 10% reduction of crystal cost

- **Large Charge Size**
  - Total charge:
    - 24” crucible: 350 ~ 400 Kg
    - 26” crucible: 500 ~ 600 Kg
  - Around 12% reduction of crystal cost

- **Diamond wire slicing**
  - Around 13% increase of wafer output
  - > 0.6 Yuan/piece reduction of wafer cost
Challenges from Mono-Si on Cost Performance

- The main cost difference between mono and multi modules/cells is caused by the cost of wafers.
- For the current efficiency difference between mono and multi (19.9% vs. 18.4%), if the cost difference is less than about 0.6-0.7 Yuan/pc, mono will have a better cost performance.
- China's “Top Runner” program is more beneficial to mono's market.
- Multi-c-Si wafers need significant technology progress to keep the competitiveness over mono wafers.

Price tendency of mono and multi wafer from 2015

Relationship between cell efficiency difference and wafer cost difference of mono and multi
What to Do for DSS (multi-) Technology Development?

- Reduce wafering cost by implementing diamond wire slicing technology.
- Utilize black silicon technology (texturing) on DWS wafers.
- Perfect the cast mono-crystalline silicon technology and commercialize quasi-mono wafers.
- Further improve mc-Si wafer quality for PERC cell technology.
- Cast bigger ingots to lower down ingot cost.
Roadmap of GCL Multi-Wafer Efficiency

- **S2**: +0.4~0.5%
- **S3**: +0.5~0.6%
- **S4**: +0.6~0.7%
- **Sp (PERC-suitable mc-Si wafer)**: +1.2~1.6%
- **Sh (Black silicon mc-Si wafer)**: +0.8~1.0%
- **Quasi-monocrystalline wafer**: +1.8~2.0%

Baseline of conventional mc-Si wafer

- 2012
- 2013
- 2015
- 2017
- 2018
More than 90% mono wafers are sliced with diamond wire saws.

DWS will be utilized soon in large scale with the help of black silicon texturing.

DWS special machine
- Capacity: 23MW
- Price: 2 ~ 3 Million Yuan

DWS mc-Si wafer
- Around 17% increase of wafer output per unit weight.
- Around 15% (0.4-0.6 Yuan/pcs) reduction of wafer cost.
GCL will soon have pre-textured DWS wafers for the market.

<table>
<thead>
<tr>
<th></th>
<th>Dry ( RIE )</th>
<th>Wet ( MCCE )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical maturity</td>
<td>Industrialization, grown and stable process and equipment.</td>
<td>In early stage of commercialization.</td>
</tr>
</tbody>
</table>
| Power increasing  | Efficiency: +0.4~0.6%  
Power: +4~5W                                                        | Efficiency: +0.2~0.4%  
Power: +2.5~4W                                                              |
| Cost             | High equipment investment and high operation cost (10-15 million Yuan/100MW), the earning at module side almost equals to operation cost. | Lower equipment investment (3-4 million Yuan/100MW), the cost is better than RIE if the output power can be increased by 2.5W. |
Perfection of Quasi-Mono technology

Targets of new quasi-mono wafers (G3)

- Mono for the entire ingots (Class I ratio ≥ 95%).
- Low dislocation density, narrow efficiency distribution.

Advantage of GCL (G3) wafers

- Apply DWS and sc-Si cell technologies directly.
- Average efficiency close to Cz wafers (∆η < 0.5%).
- Wafer cost increasing ≤ 0.15 Yuan/Pcs.
- LID the same as mc-Si cells.

Improvement on furnace
Efficiency difference compared to mono:

Surface: 0.5%

Defects in crystal: 0.2-1.2%

Further Improve Mc-Si Wafers

Cell efficiency distribution by a whole mc-Si ingot

Wide distribution, >0.6% disperse

Efficiency difference between multi and mono cells

- 1st generation
- 2nd generation
- 3rd generation
- 4th generation
Brand new co-doping technology

- Completely solving LID problem for multi-cell, and
- Providing optimized mc-Si wafers for PERC
GCL S4 Mc-Si Wafer: Low LID

Test condition: Light Power: 1000W, Height ≤70cm, 24h Exposure, Temperature: 50 ±15°C

Correction with reference cell of non-LID

Average LID value of S4 cell was around 0.01%
Average LID value of normal high efficiency multi-cell was around 0.9%-1.0%
Ratio of > 270Wp modules: increased from 23% to 78%
PERC Cells Markets: needs better mc-Si wafers

- PERC cell market is growing rapidly. The capacity is more than 12GW by now.
- Mono-Si wafers are preferred currently.
- Better mc-Si wafers are needed for PERC.
- PERC+Black silicon+DWS: cost increasing 0.2 Yuan/pcs, gaining from power increasing 1.2 Yuan/pcs, saving 0.2 Yuan/W!

**Target for mc-Si wafer for PERC:**
- More efficiency improvement (>1.0%).
- Narrower distribution of cell efficiency (0.4-0.5%).

**Hope for mc-Si:**
- PERC mass production + Black silicon: 20.5% (Jinko).

Chart from “PV Magazine”, 09/2015
Cost Reduction: Bigger mc-Si ingots

- The key technology behind the cost competitiveness of ingot casting.
- Roadmap has been bigger ingots. G8 will be more utilized in 3 years.

<table>
<thead>
<tr>
<th>Year</th>
<th>G5 furnace</th>
<th>G6 furnace</th>
<th>G7 furnace</th>
<th>G8 furnace (E)</th>
</tr>
</thead>
<tbody>
<tr>
<td>~2012</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charge: 480 KG</td>
<td>Charge: 850~880 KG</td>
<td>Charge: 1100~1200 KG</td>
<td>Charge: 1500~1600KG</td>
</tr>
<tr>
<td></td>
<td>Yield: 63.0%</td>
<td>Yield: 69%</td>
<td>Yield: 70%</td>
<td>Yield: 72%</td>
</tr>
<tr>
<td></td>
<td>Period: 63 h</td>
<td>Period: 82 h</td>
<td>Period: 90 h</td>
<td>Period: 96 h</td>
</tr>
<tr>
<td></td>
<td>Unit output: 7.6 Kg/h</td>
<td>Unit output: 10.3 Kg/h</td>
<td>Unit output: 12.4 Kg/h</td>
<td>Unit output: 16 Kg/h</td>
</tr>
<tr>
<td></td>
<td>Energy consumption: 8 Kw h/kg</td>
<td>Energy consumption: 7.5 Kv h/kg</td>
<td>Energy consumption: 7 Kw h/kg</td>
<td>Energy consumption: 6.5kw·h/kg</td>
</tr>
<tr>
<td></td>
<td>Cost: ---</td>
<td>Cost: 17% less than G5</td>
<td>Cost: 12% less than G6</td>
<td>Cost: 6% less than G7</td>
</tr>
</tbody>
</table>
Size Standardation of Mc-Si Wafers

- The same as mono M2 product, the size of multi-wafer can currently be standardized to 156.75±0.25mm. The value chain should promote this standard.
- Mc-Si wafers size can be easily increased without much cost increase. This advantage should be explored.

<table>
<thead>
<tr>
<th>Product</th>
<th>(mm) Edge Distance</th>
<th>(cm²) Effective Area</th>
<th>(cm²) Area Increase</th>
<th>(W) Wp Increase/60-cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular</td>
<td>156.0</td>
<td>243.32</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>D1</td>
<td>156.75</td>
<td>245.67</td>
<td>2.35(0.96%)</td>
<td>2.6</td>
</tr>
<tr>
<td>D2</td>
<td>158.75</td>
<td>251.98</td>
<td>8.66(3.56%)</td>
<td>9.4</td>
</tr>
</tbody>
</table>
Significant improvement of the cost performance of multi-crystalline silicon wafer is needed to keep the leading market position of mc-Si wafers.

Diamond wire slicing plus black silicon (texturing) will soon be commercialized and boost mc-Si market.

Quasi-monocrystalline technology will be revived and further developed. The cost performance of ingot casting technology can be improved significantly through quasi-mono wafers.

The continued development of mc-Si growth technology will enhance the cell efficiency of mc-Si products. The S4 product of GCL delivers low LID and increase the power output of modules.

Ingot casting cost can be further reduced by casting bigger mc-Si ingot.
Thanks for your attention!