Copper Plating Equipment for mass production of High Efficiency Silicon Solar Cells

Meco Equipment Engineers BV
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Presentation outline

• Company Introduction Besi – Meco
• Why using plating?
• Processes Direct Plating Line (DPL)
• Results obtained up to now
• Cost-of-ownership copper plating process
• Summary and conclusions
Meco as part of Besi NV

BESI Group:

• Leading Assembly Equipment Supplier for semiconductor back-end industry
• Revenue : 254.9 M€ (2013)
• Employees : 1600 fte (WW)
• Sales & Support operations : China, Korea, Taiwan, Philippines, Malaysia and Singapore
• Production : 7 Locations (incl. Asia)

Die Attach Equipment Product Group
Packaging Equipment Product Group

Wire Bonding Equipment Product Group
Plating Equipment Product Group (Market share > 50%)
### Why using plating?

<table>
<thead>
<tr>
<th></th>
<th>Ag screen print</th>
<th>Ni/Cu/Sn Plating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower material cost</td>
<td>Ag price US$ 550/kg</td>
<td>Cu price US$ 7/kg</td>
</tr>
<tr>
<td>Narrow line width</td>
<td>50 – 120 μm</td>
<td>20 - 40 μm</td>
</tr>
<tr>
<td>• Reduced shading or</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Reduced emitter resistance loss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower resistivity</td>
<td>3-10 μΩ.cm</td>
<td>1.7 μΩ.cm</td>
</tr>
<tr>
<td>Lower contact resistance</td>
<td>Highly sensitive to firing temperature</td>
<td>~ 0.1 mΩ.cm²</td>
</tr>
<tr>
<td>Higher aspect ratio (h:w)</td>
<td>Range 1:10 to 1:2</td>
<td>1:2 (higher with resist mask)</td>
</tr>
<tr>
<td>Lower firing temperature</td>
<td>750 – 800 °C</td>
<td>350 – 400 °C</td>
</tr>
</tbody>
</table>
CPL & DPL SOLAR
Electric plating directly onto silicon

- Adding LED light / Back side cell contact
- Direct plating on FS silicon or seed layer

- Front side contact on seed layer
- Standard high speed electro-plating
CPL & DPL SOLAR
Schematic plating concept

Plating channel cross section

Requirement for electro-plating:
Robust / reproducible electrical contact

Cathode (Contact Belt)
Running direction
Plating chemistry
Soluble Anode
CPL & DPL SOLAR

Loading to contact belt

- Loading from slotted cassette
- Buffering of multiple cassettes
- Tracking of individual wafers

- Unloading side can be connected to cell sorter
- Buffering (in case machine needs to run empty)
- Processed wafers can optionally be loaded into cassettes
CPL & DPL SOLAR
Features Meco CPL & DPL

- Vertical product handling
- Low Drag Over of chemistry
- High bath agitations possible as wafers are fixed in belt
- High deposit speed (15 - 20 ASD)
- Matured machine concept, > 375 lines for semicon in Asia running 24/7
- Contact belt well proven; cleaned without affecting tool uptime
- Low breakage rates < 0.10%, proven down to 120 um wafers
- Front & backside plating possible (e.g. for IBC cells and bi-facial cells such as HIT)
- 50 – 100 MW per line
CPL & DPL SOLAR
Contact belt – Customizable to your cell design

Front side Plating
Bifacial Plating (HIT Cells)
LIP directly onto Silicon
DPL SOLAR
Electrolytic plating directly onto silicon

- Very fine contact fingers (< 35 µm after plating)
- Reduced shading leads to efficiency increase up to + 1%
- Plating process is self-aligning
- Front side screen printing can be eliminated
- Achieved $\eta = 20.5\%$ (average value), $\eta = 20.8\%$ (record cell)
DPL SOLAR
Direct metallization process sequence DPL

SiN_x opening
Laser / wet etching

SiO_2 removal
(HF)

LIP Ni

NiSi_x formation
(annealing)

LIP Cu

Cu plating

Ag or Sn plating

Annealing: NiSi_x formation:
• Contact resistance
• Peel strength
• Process conditions
• Process sequence
STD PERC processing up to firing (local Al-BSF formation)

ps-UV laser ablation SiO$_2$/SiNx ARC
DPL SOLAR

STD PERC processing up to firing (local Al-BSF formation)

ps-UV laser ablation SiO$_2$/SiNx ARC

LIP Ni

SiN$_x$
SiO$_2$

n+:
Rsh~120Ω/

Rear dielectrics

~12 um
DPL Solar

Front side cu based process sequence step2

STD PERC processing up to firing (local Al-BSF formation)

ps-UV laser ablation SiO$_2$/SiN$_x$ ARC

- LIP Ni
- Cu
- Thin immersion Ag

Rear dielectrics

SiN$_x$
SiO$_2$
n+:
Rsh$\sim$120Ω/□

25 - 35 μm
Front side cu based process sequence step3

STD PERC processing up to firing (local Al-BSF formation)

ps-UV laser ablation SiO₂/SiNx ARC

LIP Ni

Cu

Thin immersion Ag

Rapid thermal annealing (N₂)

Nickel silicide contact

Rsh~120Ω/□
Large wafer batch I-V results

**Average I-V results (0.5μm emitter, front grid optimized)**
156x156 mm², CZ-Si, p-type, 160 μm thick, 1-3 Ω.cm
(only 1 electrical failure excluded)

<table>
<thead>
<tr>
<th></th>
<th>$j_{sc}$ [mA/cm²]</th>
<th>$V_{oc}$ [mV]</th>
<th>FF [%]</th>
<th>η [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average</td>
<td>38.8</td>
<td>661.3</td>
<td>80.0</td>
<td>20.5</td>
</tr>
<tr>
<td>(109 cells)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CoV**</td>
<td>0.26%</td>
<td>0.18%</td>
<td>0.25%</td>
<td>0.49%</td>
</tr>
<tr>
<td>Best cell</td>
<td>39.1</td>
<td>661.7</td>
<td>80.0</td>
<td>20.7*</td>
</tr>
</tbody>
</table>

**Coefficient of variation = standard deviation/mean (%)**

*Externally confirmed at FhG-ISE CalLab

- Average eta >20.5%
- Excellent FF~80.0%
- Very narrow distribution with all cells >20%
- N-Type : > 21.5%
Large wafer batch I-V results

FF values (%) for 109 Cu plated cells

Voc values (mV) for 109 Cu plated cells
Maximum ribbon pull force values at 45° pull angles for both emitters tested (presented by IMEC at 28th EU PVSEC Conference)
DPL SOLAR
10 cell string mini module data

IEC61215 test pass criterion is < 5% Pmax loss after 200 thermal cycles (-40 to 85 deg C) or 1000 hours damp heat exposure (85 deg C, 85% relative humidity)

<table>
<thead>
<tr>
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<th>IEC61215</th>
<th>Extended IEC61215</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>200 Thermal cycles</td>
<td>1000 Hrs Damp Heat</td>
</tr>
<tr>
<td>3 Cu 10 cell strings Conductive adh.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta I_{sc}$</td>
<td>2.9%</td>
<td>2.0%</td>
</tr>
<tr>
<td>$\Delta V_{oc}$</td>
<td>0.2%</td>
<td>1.2%</td>
</tr>
<tr>
<td>$\Delta F_F$</td>
<td>-1.2%</td>
<td>-0.6%</td>
</tr>
<tr>
<td>$\Delta \text{Eff}$</td>
<td>1.9%</td>
<td>2.7%</td>
</tr>
<tr>
<td>Max $\Delta \text{Eff}$</td>
<td>0.9%</td>
<td>0.6%</td>
</tr>
</tbody>
</table>

| 2 Ag 10 cell strings 1 Conductive adh. 1 std. solder | | | |
| $\Delta I_{sc}$ | 1.6% | 1.7% | 0.5% | 1.5% |
| $\Delta V_{oc}$ | 0.2% | 0.3% | 0.2% | 0.3% |
| $\Delta F_F$   | -0.8% | 0.5% | -0.7% | -0.4% |
| $\Delta \text{Eff}$ | 0.9% | 2.3% | -0.2% | 1.5% |
| Max $\Delta \text{Eff}$ | 0.9% | 1.8% | -0.2% | 0.7% |
DPL SOLAR

Front side metallization: CoO model

- Meco DPL – 1 µm LIP Ni – 10 µm Cu - 0.3 µm Ag)
- Based on 1,500 wph production line

Screen printing process Ag paste = 0.023 US$/Wp (Ag : 21 US$/oz.)

Direct plate Ni – Cu – Ag = 0.017 US$/Wp

Wafer-to-cell conversion cost:
- excl. silicon raw material
- incl. BS screen = 0.05 US$/Wp

Cell efficiency increase: 0.76%, leading to 2.33 MW added output

Cost savings: 0.0125 US$/Wp (on front side metallization only !)
CPL & DPL SOLAR

Summary

• Electroplating with Meco CPL & DPL is cost effective (ROI: 9-20 months based on ASP of 0.5 US$/Wp)

• + 0.3 - 0.5% cell efficiency improvement with fine line printing + Meco CPL

• + 0.7 – 1.0% efficiency improvement can be achieved when using laser opening of SiNx layer + Meco DPL; metallization onto high Ohmic emitters feasible (100 – 120 Ω / □)

• 20.8 % efficiency achieved with Meco DPL (front side H-pattern, p type); on HIT and IBC cells 23-24 % efficiency achieved.

• Strong cost reductions: ~ 0.0125 US$/Wp (on frontside) with DPL Ni-Cu-Sn plating; with bi-facial cells and HIT cells more cost reduction feasible

• Output of Meco CPL or DPL is 50 - 100 MW based on 95% uptime

• Meco CPL is the ideal metallization platform for IBC, HIT and n-type cells

• Freedom of choice in plating metals (Ag or Ni,Cu,Sn)

More power at a lower cost
Thank you, 謝謝
Meet us in booth # A0118